

FIG. 1 DIAGRAM FOR EXPLAINING PRINCIPLE OF PRESENT INVENTION

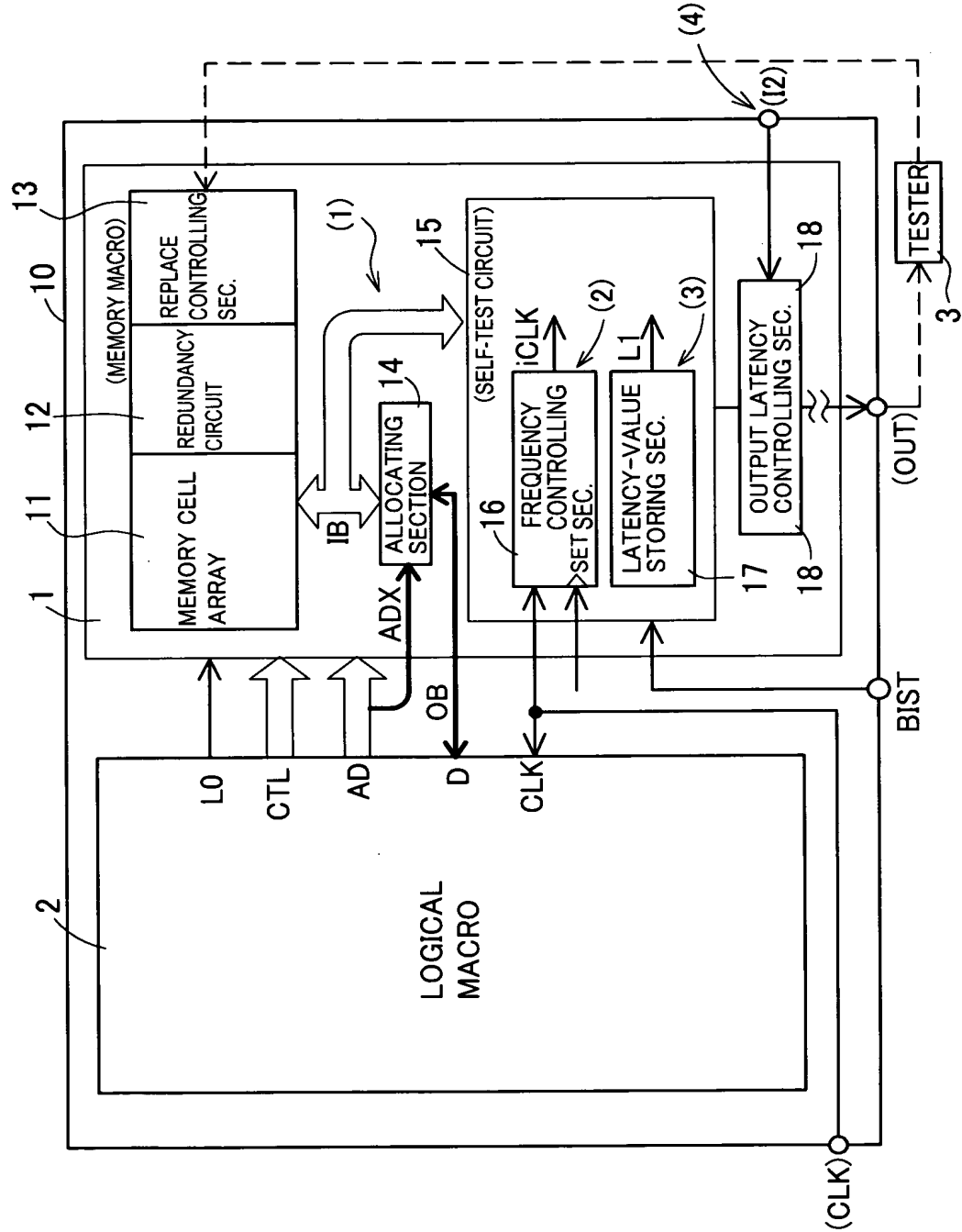


FIG. 2

CIRCUIT BLOCK DIAGRAM DIRECTED TO FIRST EMBODIMENT

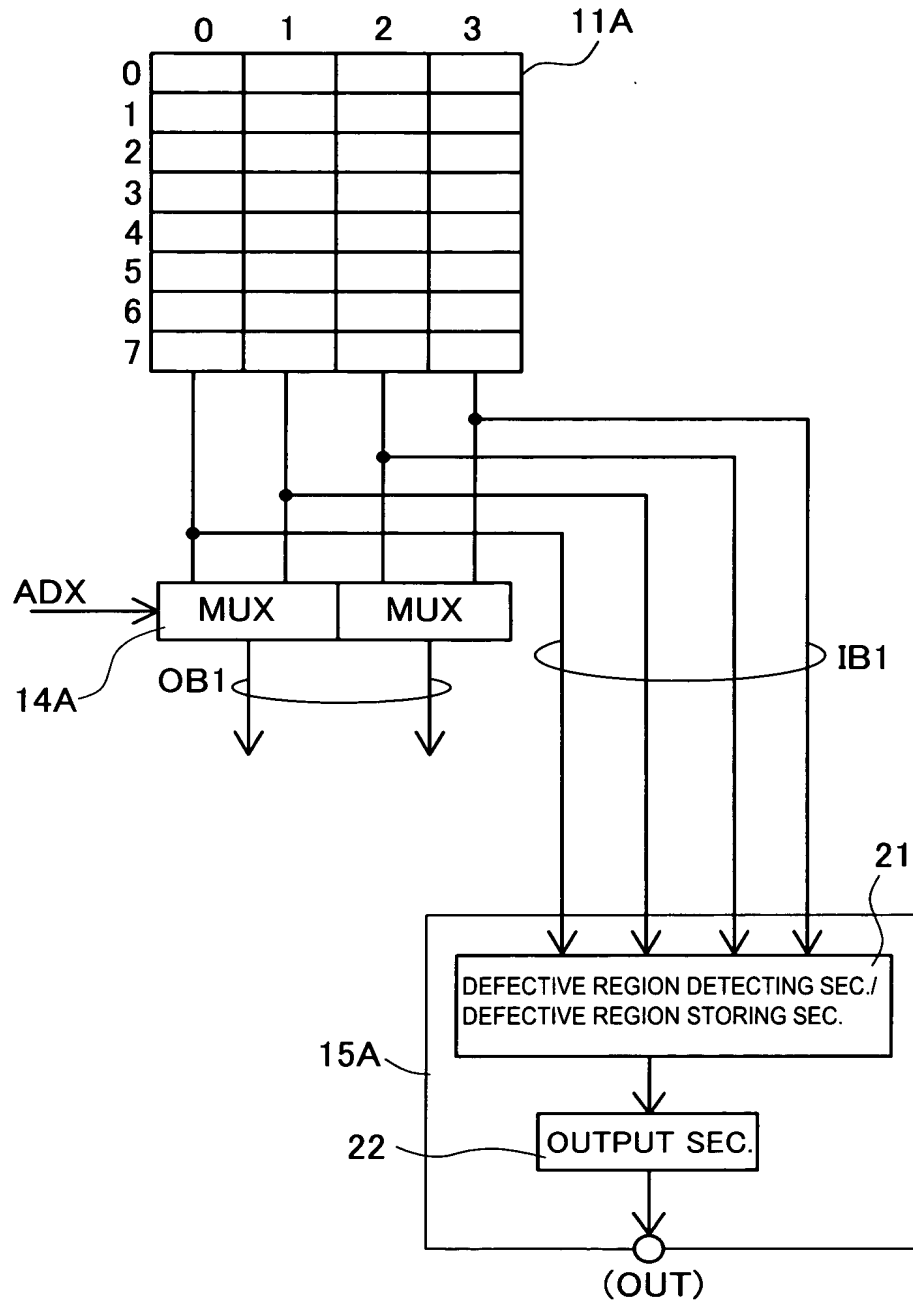


FIG. 3

CIRCUIT BLOCK DIAGRAM DIRECTED TO SECOND EMBODIMENT

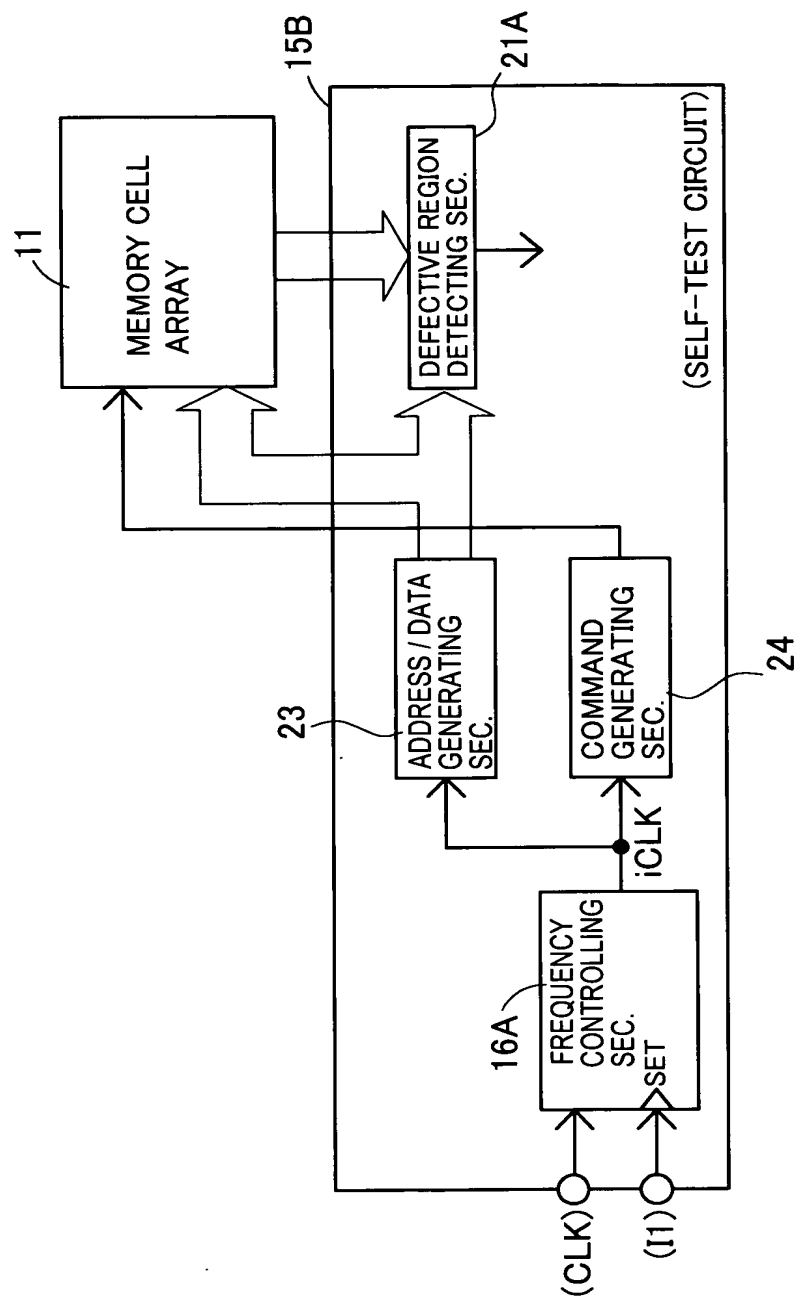


FIG. 4 SPECIFIC EXAMPLE OF FREQUENCY CONTROLLING SECTION

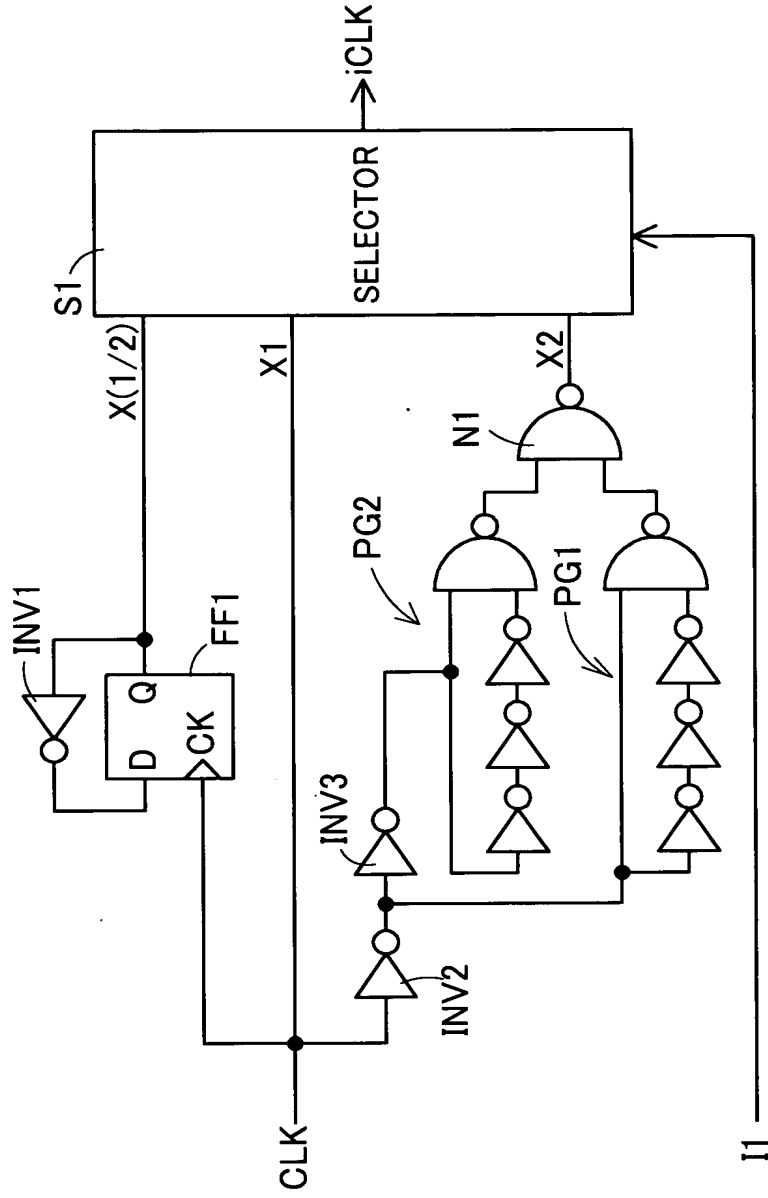
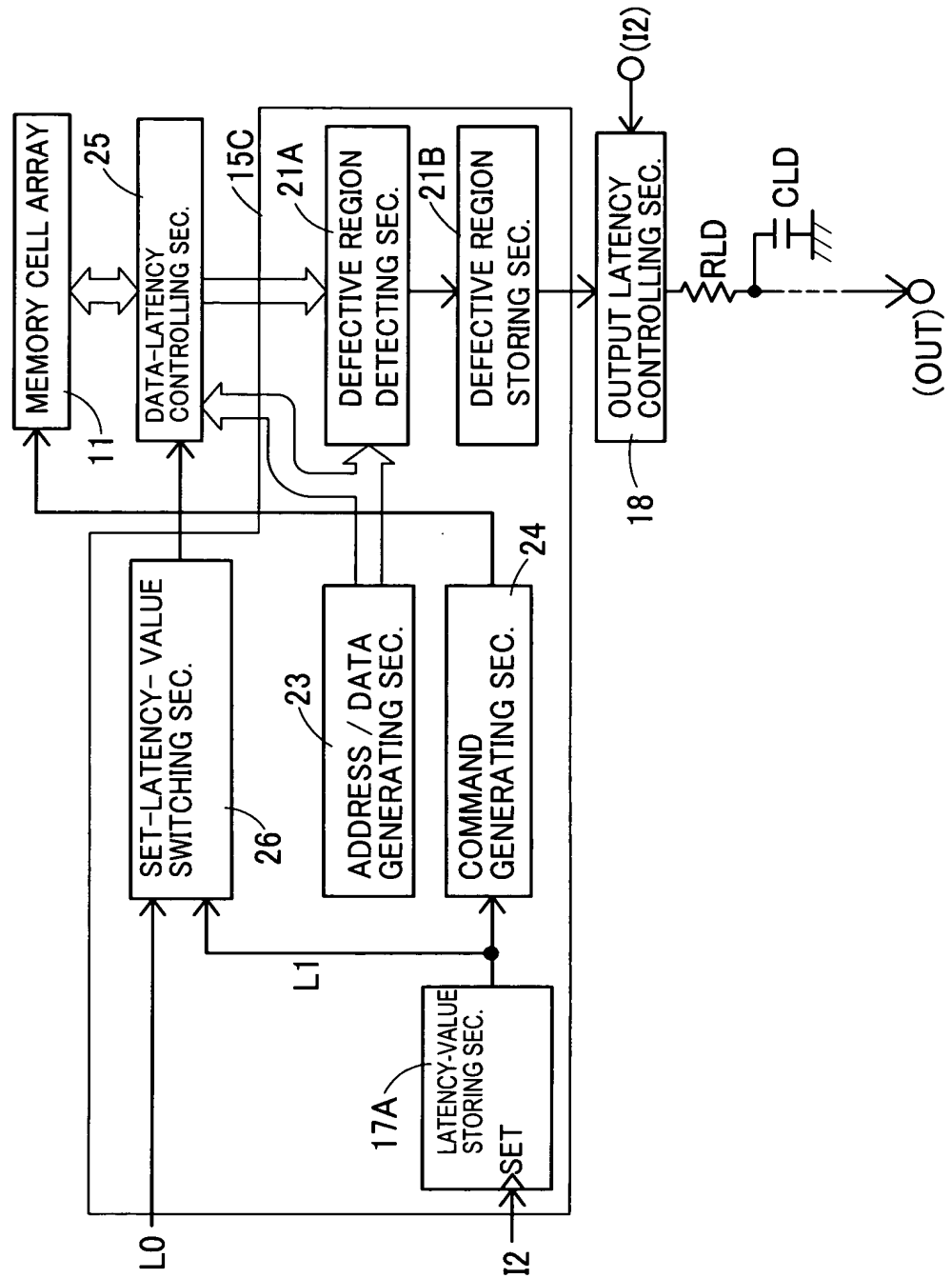


FIG. 5 CIRCUIT BLOCK DIAGRAM DIRECTED TO THIRD EMBODIMENT



Title: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE
AND SELF-TEST METHOD OF MEMORY MACRO
Inventor's Name: Katsuhiko ITAKURA
Application No.: New Application
Docket No.: 024016-00070

FIG. 6

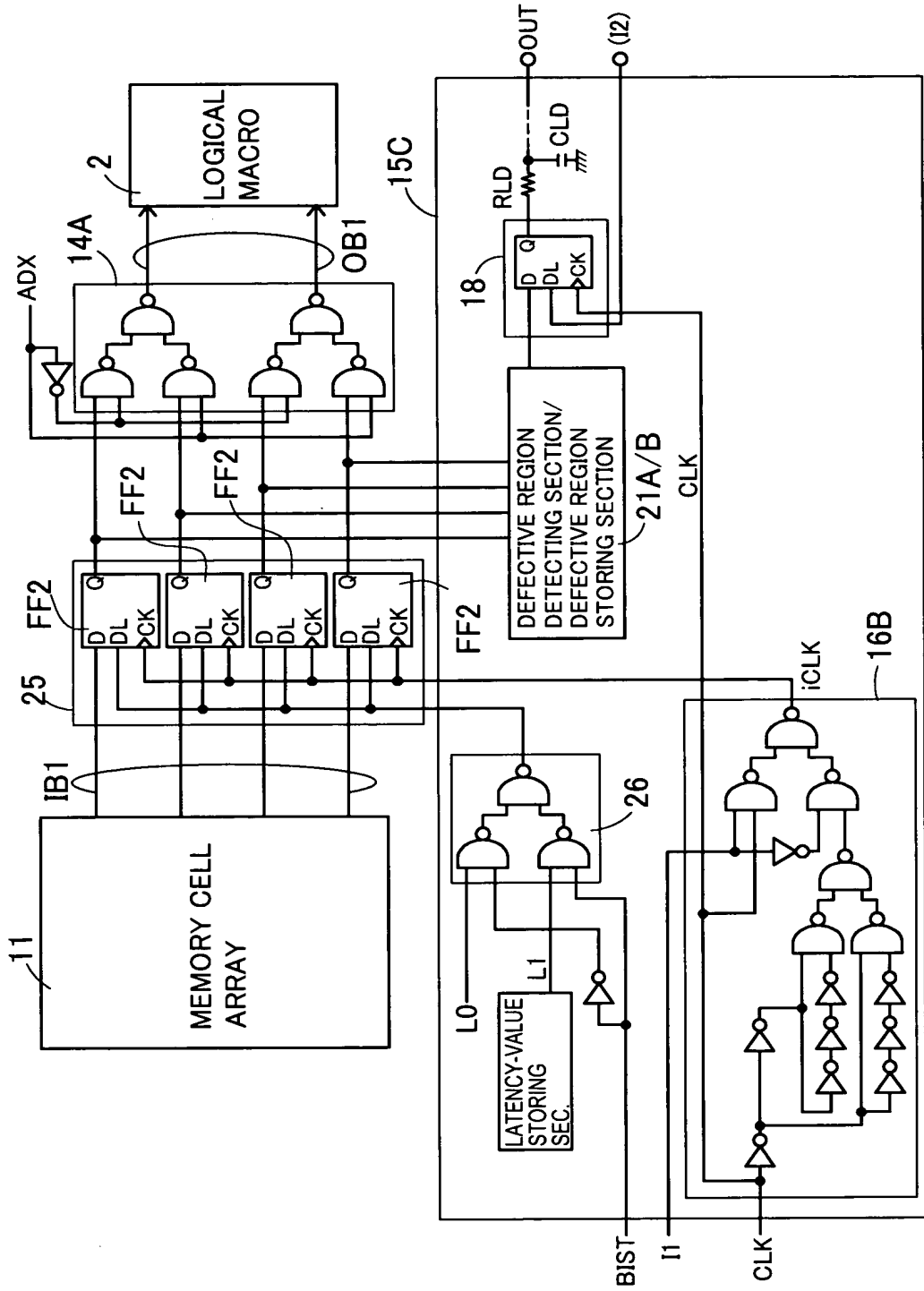


FIG. 7

SPECIFIC EXAMPLE OF DATA-LATENCY CONTROLLING SECTION
(FOR ONE-BIT DATA)

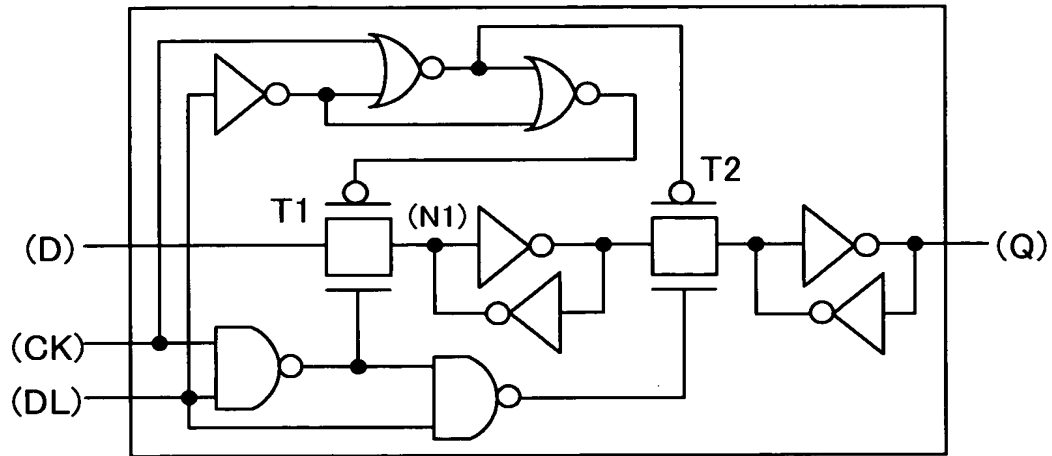


FIG. 8

OPERATIONAL WAVEFORM DIAGRAM OF CASE THAT LATENCY 2
(DL="H") IS SET FOR FIG. 7

(DL="H")

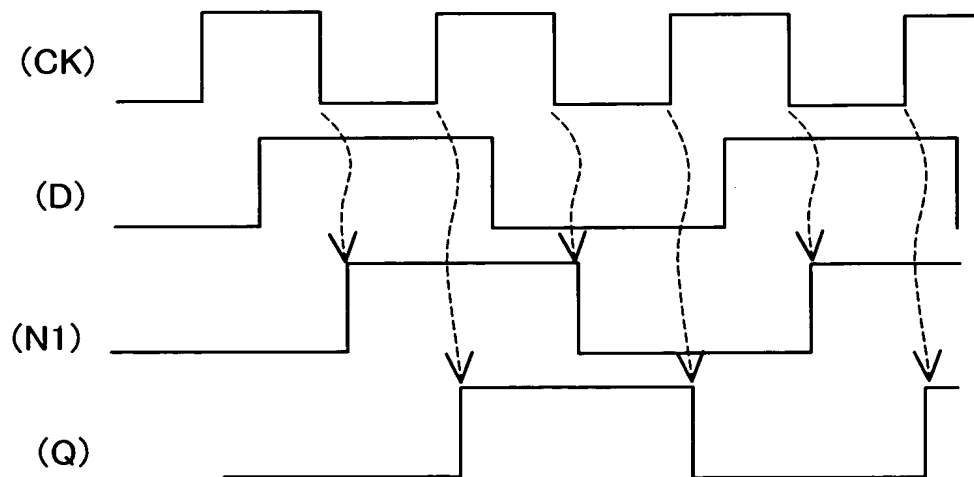


FIG. 9

CIRCUIT BLOCK DIAGRAM DIRECTED TO FOURTH EMBODIMENT

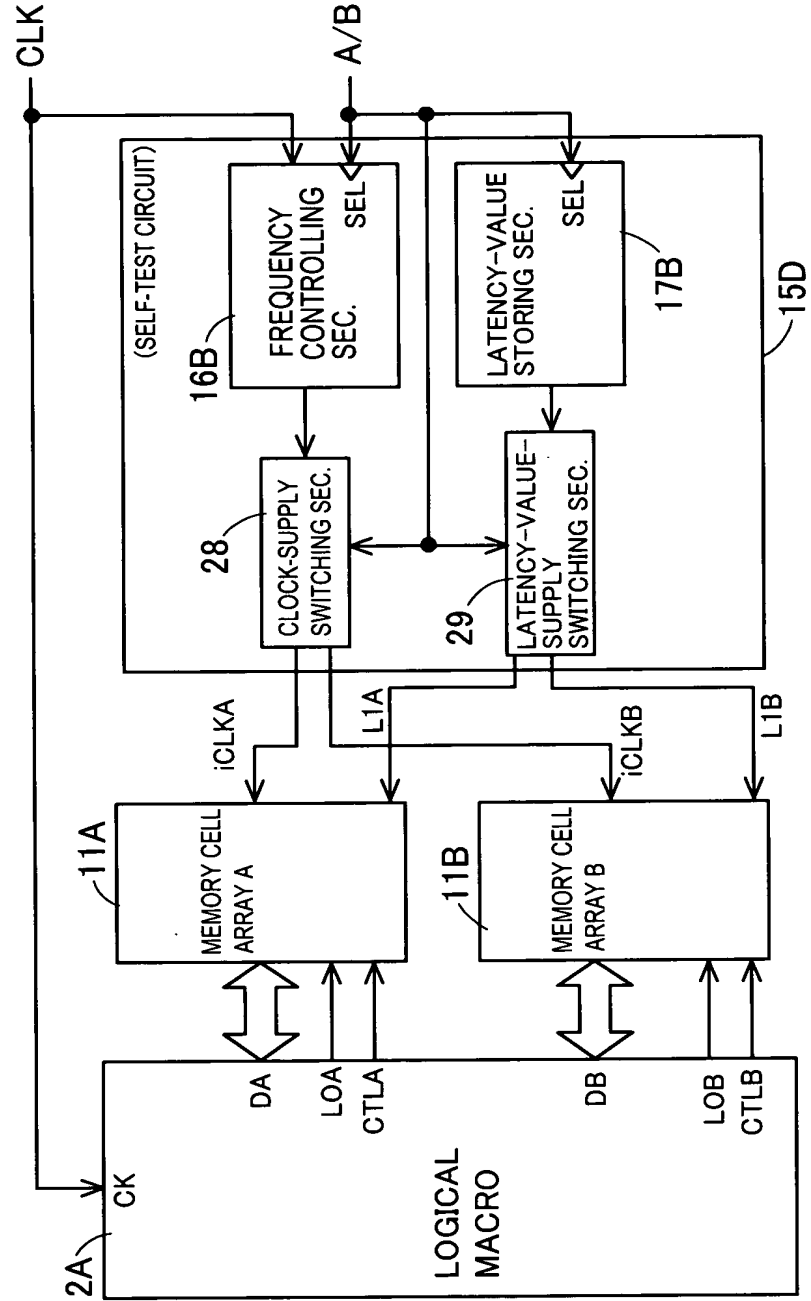


FIG. 10 PRIOR ART

CIRCUIT BLOCK DIAGRAM OF CONVENTIONAL SELF-TEST CIRCUIT

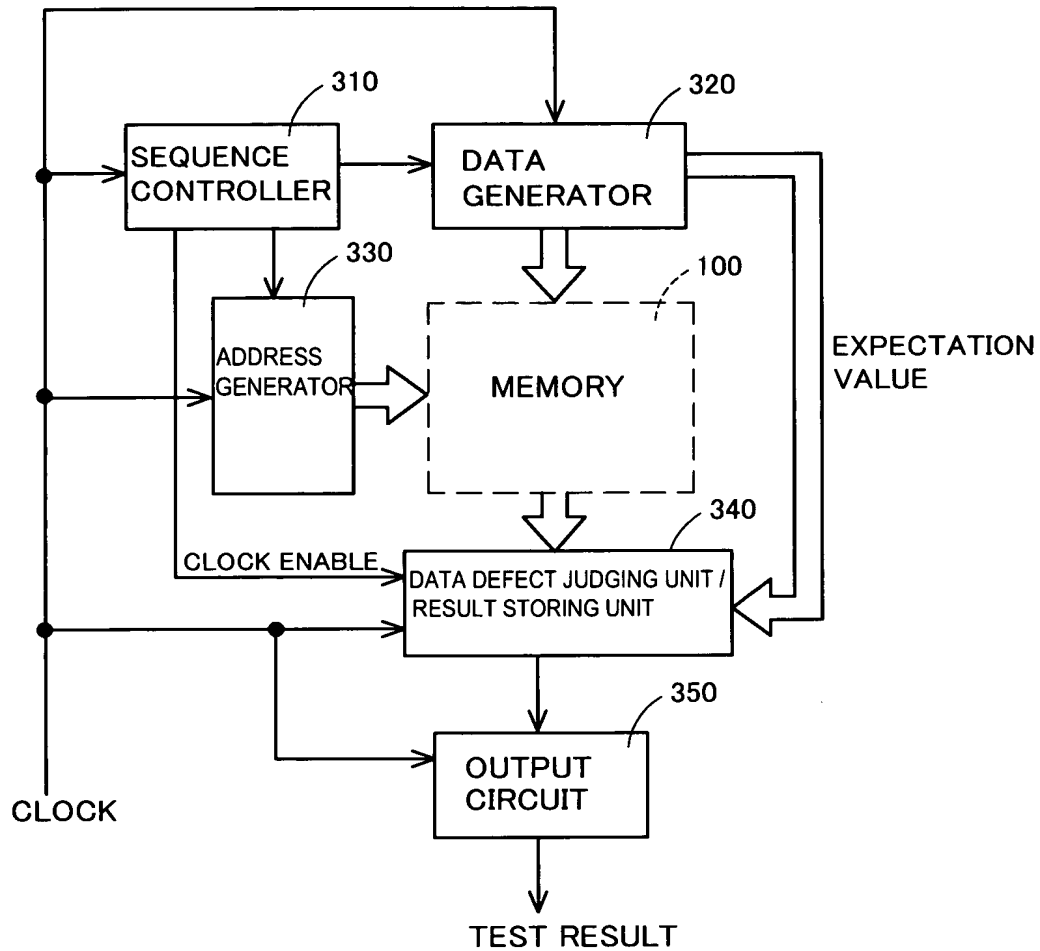


FIG. 11

CONCEPTUAL DIAGRAM SHOWING DIFFERENCE OF REDUNDANCY STRUCTURE
THAT DIFFERS BY LOGICAL ADDRESS SPACE IN MEMORY CELL ARRAY

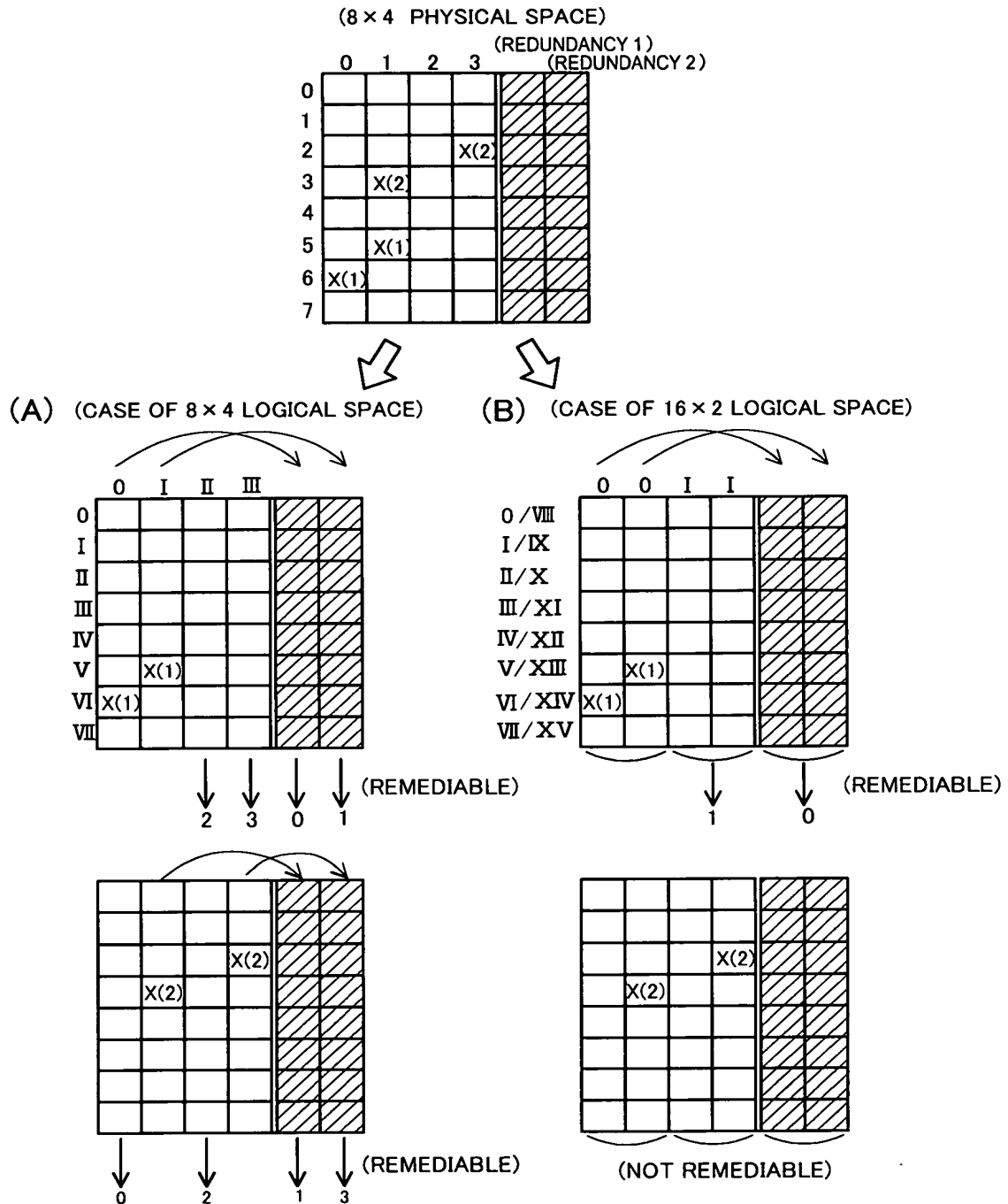
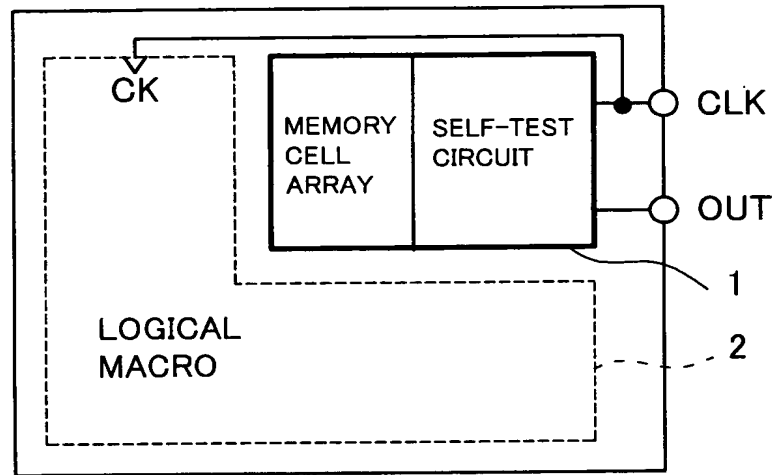


FIG. 12

CONCEPTUAL DIAGRAM SHOWING LAYOUT OF MEMORY MACRO
AND EXTERNAL TERMINALS OF SEMICONDUCTOR INTEGRATED
CIRCUIT DEVICE

(A) SHORT FROM PAD TO MEMORY



(B) LONG FROM PAD TO MEMORY

